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| Substitute for form 1449A/PTO | | | | Complete if Known | |
| INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary) | | | | Applicant Number | Not yet assigned |
| | | | | Filing Date | Herewith |
| | | | | First Named Inventor | KESHAVARZI, Ali |
| | | | | Group Art Unit | Not yet assigned |
| | | | | Examiner Name | Not yet assigned |
| Sheet | 1 | of | 1 | INTEL Docket Number | P18062 |

| OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS | | | | |
|---|-----------------------|---|----------------|--|
| Examiner Initials* | Cite No. ¹ | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. | T ² | |
| TTN | A | Ohsawa, Takashi et al., "Memory Design Using a One-Transistor Gain Cell on SOI, IEEE Journal of Solid-State Circuits, Vol. 37, No. 11, November 2002, ISSN: 0018-9200, pp. 1510-1522. | | |
| TTN | B | Thompson, Scott, et al., "MOS Scaling: Transistor Challenges for the 21 st Century", Intel Technology Journal Q3'98. 19pgs. | | |
| TTN | C | Ohsawa, Takashi et al., "ISSCC 2002/Session 9/Dram and Ferroelectric Memories / 9.1", Memory LSI Research and Development Center, Yokohama, Japan. 3pgs. | | |
| TTN | D | Brand, A., "Intel's 0.25 Micron, 2.0Volts Logic Process Technology", Intel Technology Journal Q3'98. 9pgs. | | |
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| Examiner Signature |  | Date Considered | 8/5/05 |
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹Unique citation designation number. ²Applicant is to place a check mark here if English language Translation is attached.